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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/870,280	SHAKERI ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9, 11-36 were examined.

Section I: Prosecution is Reopened

2. Based on the pre-appeal brief discussion, prosecution is hereby reopened. An action on the merits appears below.

Section II: Non-Final Rejection

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-7,11-14,16-26, 28-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Dwan et al., titled, "Introducing Simulink into a Systems Engineering Curriculum" (1993); hereafter Dwan. Dawn teaches simulating linear/non-linear dynamic systems

Claim 1. A modeling process (i.e., simulation, pg. 627, Preliminaries section) comprising: providing a plurality of blocks (the teaching of manipulating a plurality of blocks, pg.627, "To Manipulate Blocks" section paragraphs 1-3), each of the blocks representing functional entities (disclosure defines functional entities pg.6, lines 19-23 as a function that operates signal values to which pg.630 figure 2 "sum" teaches)

that operate on a plurality of input signal values (signal values from the signal generator, pg. 630, right column, figure 1); generating a plurality of output signal values ("plot your results in MATLAB after checking 'whos' to see all your outputs", pg.630, section 4. "Results" section, 1st paragraph) (pg.628, right column, "To interconnect the blocks" section) from the plurality of blocks (the teaching of manipulating a plurality of blocks, pg.627, "To Manipulate Blocks" section paragraphs 1-3); grouping the plurality of output signal values ("plot your results in MATLAB after checking 'whos' to see all your outputs", pg.630, section 4. "Results" section, 1st paragraph) (pg.628, right column, "To interconnect the blocks" section) as an ordered set in a multiplexer (pg.628, right column, "To interconnect the blocks" section, "mux")as a first composite signal (pg.631, figure 5 output of the "sum" block, to which the disclosure, pg.7, lines 15-17, states, "a composite represents an ordered set of signals that are bundled together..."); outputting the first composite signal (pg.631, figure 5 output of the"sum" block, to which the disclosure, pg.7, lines 15-17, states, "a composite represents an ordered set of signals that are bundled together..."); and storing the first composite signal (pg.631, figure 5 output of the"sum" block, to which the disclosure, pg.7, lines 15-17, states, "a composite represents an ordered set of signals that are bundled together...") in a storage device (inherency since software is stored on a disk, computer etc.).

Claim 2. The process of claim 1 wherein each of the blocks includes at least one

input signal port (pg.628, left column, 4th paragraph, "input port", with pg.630, figure 2, "step form") and at least one output signal port (pg.628, left column, 4th paragraph, "output port", with pg.630, figure 2, "step form").

Claim 3. The process of claim 1 wherein the input signal values (signal values from the signal generator, pg. 630, right column, figure 1) and the output signal values ("plot your results in MATLAB after checking 'whos' to see all your outputs", pg.630, section 4. "Results" section, 1st paragraph) have at least one attribute.

Claim 4. The process of claim 3 wherein the attribute is a name (pg.627, left column, "The Windows Environment" section, point 3, 'click on the title block of the window"; pg.630, figure 4, "clock").

Claim 5. The process of claim 3 wherein the attribute is a data type (example, pg.630, figure 3, "transfer form") .

Claim 6. The process of claim 3 wherein the attribute is a numeric type (example, pg.629, right column, lines 1-10, list of numeric parameters) .

Claim 7. The process of claim 3 wherein the attribute is a dimensionality (2 dimensional matrix, pg.630, left column, section 4b "output matrix be a (2 x 2) matrix).

Claim 11. The process of claim 1 further comprising decomposing the first composite signal (pg.631, figure 5 output of the"sum" block, to which the disclosure, pg.7, lines 15-17, states, "a composite represents an ordered set of signals that are bundled together...")into the plurality of output signals (pg.628, left column, 4th paragraph, "output port", with pg.630, figure 2, "step form") in a demultiplexer.

Claim 12. The process of claim 1 further comprising viewing (pg.630, figure 3, "scope") the ordered set contained in the first composite signal (pg.631, figure 5 output of the"sum" block, to which the disclosure, pg.7, lines 15-17, states, "a composite represents an ordered set of signals that are bundled together...") with a composite signal viewer (pg.630, figure 3, "scope").

Claim 13. The process of claim 1 wherein at least one of the input signal values (signal values from the signal generator, pg. 630, right column, figure 1) is a second composite signal (pg.631, figure 5 output of the"sum" block, to which the disclosure, pg.7, lines 15-17, states, "a composite represents an ordered set of signals that are bundled together...").

Claim 14. A computer implemented block diagram modeling process (i.e., simulation, pg. 627, Preliminaries section)comprising: providing a first block and a second block, the blocks (covers a plurality of blocks, pg.627, right column, "To Manipulate Blocks" section, numbers 1-3) representing functional entities (disclosure defines functional

entities pg.6, lines 19-23 as a function that operates signal values to which pg.630 figure 2 "sum" teaches) that operate on a plurality of input signal values (signal values from the signal generator, pg. 630, right column, figure 1); generating a plurality of output signal values ("plot your results in MATLAB after checking 'whos' to see all your outputs", pg.630, section 4. "Results" section, 1st paragraph) from the first and second block(covers a plurality of blocks, pg.627, right column, "To Manipulate Blocks" section, numbers 1-3); grouping the plurality of output signal values (signal values from the signal generator to the scopes via the mux, pg. 630, right column, figure 1) as an ordered set in a multiplexer (pg.628, right column, "To interconnect the blocks" section, "mux")as a first composite signal (pg.631, figure 5 output of the"sum" block, to which the disclosure, pg.7, lines 15-17, states, "a composite represents an ordered set of signals that are bundled together..."); processing the composite signal in a third block (covers a plurality of blocks, pg.627, right column, "To Manipulate Blocks" section, numbers 1-3); and storing the composite signal in a storage device (inherency since software is stored on a disk, computer etc.).

Claim 16. The process of claim 14 wherein at least one of the input signals is a second composite signal (pg.631, figure 5 output of the"sum" block, to which the disclosure, pg.7, lines 15-17, states, "a composite represents an ordered set of signals that are bundled together...").

Claim 17. The process of claim 14 further comprising decomposing the composite

signal into the plurality of input signal values (signal values from the signal generator, pg. 630, right column, figure 1).

Claim 18. The process of claim 14 further comprising viewing the composite signal in a composite signal viewer (pg.630, figure 3, "scope").

Claim 19. The process of claim 18 wherein the composite signal viewer (pg.630, figure 3, "scope") displays the ordered set contained in the composite signal on a graphical user interface (GUI).

Claim 20. The process of claim 19 wherein the GUI(inherent to the Windows application, pg.627, "Windows Environment") is provided on an input/output device.

Claim 21. A computer program product residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to: provide a plurality of blocks (the teaching of manipulating a plurality of blocks, pg.627, "To Manipulate Blocks" section paragraphs 1-3), each of the blocks representing functional entities (disclosure defines functional entities pg.6, lines 19-23 as a function that operates signal values to which pg.630 figure 2 "sum" teaches)that operate on a plurality of input signal values (signal values from the signal generator, pg. 630, right column, figure 1); generate a plurality of output signal values ("plot your

results in MATLAB after checking 'whos' to see all your outputs", pg.630, section 4. "Results" section, 1st paragraph) (pg.628, right column, "To interconnect the blocks" section) from the plurality of blocks (the teaching of manipulating a plurality of blocks, pg.627, "To Manipulate Blocks" section paragraphs 1-3); group the plurality of output signal values ("plot your results in MATLAB after checking 'whos' to see all your outputs", pg.630, section 4. "Results" section, 1st paragraph) (pg.628, right column, "To interconnect the blocks" section) as an ordered set in a multiplexer (pg.628, right column, "To interconnect the blocks" section, "mux") as a first composite signal (pg.631, figure 5 output of the"sum" block, to which the disclosure, pg.7, lines 15-17, states; "a composite represents an ordered set of signals that are bundled together..."); and output the first composite signal (pg.631, figure 5 output of the"sum" block, to which the disclosure, pg.7, lines 15-17, states, "a composite represents an ordered set of signals that are bundled together...") and store the first composite signal (pg.631, figure 5 output of the"sum" block, to which the disclosure, pg.7, lines 15-17, states, "a composite represents an ordered set of signals that are bundled together...") in a storage device (inherency since software is stored on a disk, computer etc.).

Claim 22. The computer program product of claim 21 wherein the computer readable medium is a random access memory (RAM) (inherent to the properties of a computer; pg.627, left column, "Preliminaries" 386 processor which is stored on PC).

Claim 23. The computer program product of claim 21 wherein the computer readable

medium is read only memory (ROM) (inherent to the properties of a computer; pg.627, left column, "Preliminaries" 386 processor which is stored on PC).

Claim 24. The computer program product of claim 21 wherein the computer readable medium is hard disk drive(inherent to the properties of a computer; pg.627, left column, "Preliminaries" 386 processor which is stored on PC).

Claim 25. A processor and a memory configured to: provide a plurality of blocks (the teaching of manipulating a plurality of blocks, pg.627, "To Manipulate Blocks" section paragraphs 1-3), each of the blocks representing functional entities (disclosure defines functional entities pg.6, lines 19-23 as a function that operates signal values to which pg.630 figure 2 "sum" teaches) that operate on a plurality of input signal values (signal values from the signal generator, pg. 630, right column, figure 1); generate a plurality of output signal values ("plot your results in MATLAB after checking 'whos' to see all your outputs", pg.630, section 4. "Results" section, 1st paragraph) (pg.628, right column, "To interconnect the blocks" section) from the plurality of blocks (the teaching of manipulating a plurality of blocks, pg.627, "To Manipulate Blocks" section paragraphs 1-3); group the plurality of output signal values ("plot your results in MATLAB after checking 'whos' to see all your outputs", pg.630, section 4. "Results" section, 1st paragraph) (pg.628, right column, "To interconnect the blocks" section) as an ordered set in a multiplexer (pg.628, right column, "To interconnect the blocks" section, "mux")as a first composite signal (pg.631, figure 5 output of the"sum" block, to

which the disclosure, pg.7, lines 15-17, states, "a composite represents an ordered set of signals that are bundled together..."); output the first composite signal (signal values from the step function to the scope via the transfer function, pg. 630, right column, figure 2); and store the first composite signal (pg.631, figure 5 output of the"sum" block, to which the disclosure, pg.7, lines 15-17, states, "a composite represents an ordered set of signals that are bundled together...") in a storage device (inherency since software is stored on a disk, computer etc.).

Claim 26. The processor and memory of claim 25 wherein the processor and the memory (inherent to the properties of a computer; pg.627, left column, "Preliminaries" 386 processor which is stored on PC) are incorporated into a personal computer.

Claim 28. The processor and memory of claim 25 wherein the processor(inherent to the properties of a computer; pg.627, left column, "Preliminaries" 386 processor which is stored on PC) and the memory are incorporated into a single board computer.

Claim 29. A modeling process (i.e., simulation, pg. 627, Preliminaries section)comprising: providing a plurality of blocks (the teaching of manipulating a plurality of blocks, pg.627, "To Manipulate Blocks" section paragraphs 1-3), each of the blocks representing a functional entity that operates on one or more input signal values and generates one or more output signals; grouping the output

signals use an ordered set in a multiplexer (pg.628, right column, "To interconnect the blocks" section, "mux")as a composite signal; outputting the composite signal; and storing the composite signal in a storage device (inherency since software is stored on a disk, computer etc.).

Claim 30. The process of claim 29 wherein the ordered set is a tree data structure (an example of a data structure, 2 dimensional matrix, pg.630, left column, section 4b "output matrix be a (2 x 2) matrix).

Claim 31. The process of claim 30 wherein the tree data structure (an example of a data structure, 2 dimensional matrix, pg.630, left column, section 4b "output matrix be a (2 x 2) matrix) is a linked list.

Claim 32. The process of claim 29 further comprising: providing a composite signal viewer; and viewing the ordered set in a graphical user interface (inherent to the Windows application, pg.627, "Windows Environment") executing in the composite signal viewer (pg.630, figure 3, "scope").

Claim 33. A computer program product residing on a computer readable medium having instructions stored thereon which, when executed by the processor, cause the processor to: provide a plurality of blocks (the teaching of manipulating a plurality of blocks, pg.627, "To Manipulate Blocks" section paragraphs 1-3), each of the blocks

representing a functional entity that operates on one or more input signal values (signal values from the signal generator, pg. 630, right column, figure 1) and generates one or more output signal values ("plot your results in MATLAB after checking 'whos' to see all your outputs", pg.630, section 4. "Results" section, 1st paragraph); group the output signals as an ordered set in a multiplexer (pg.628, right column, "To interconnect the blocks" section, "mux")as a composite signal; output the composite signal; and store the composite signal in a storage device (inherency since software is stored on a disk, computer etc.).

Claim 34. A processor (inherent to the properties of a computer; pg.627, left column, "Preliminaries" 386 processor which is stored on PC) and memory configured to provide a plurality of blocks (the teaching of manipulating a plurality of blocks, pg.627, "To Manipulate Blocks" section paragraphs 1-3), each of the blocks representing a functional entity that operates on one or more input signal values (signal values from the signal generator, pg. 630, right column, figure 1) and generates one or more output signal values ("plot your results in MATLAB after checking 'whos' to see all your outputs", pg.630, section 4. "Results" section, 1st paragraph); group the output signals as an ordered set in a multiplexer (pg.628, right column, "To interconnect the blocks" section, "mux")as a composite signal; output the composite signal; and store the composite signal in a storage device (inherency since software is stored on a disk, computer etc.).

Claim 35. A method for providing a composite signal in a modeling environment, the method (i.e., simulation, pg. 627, Preliminaries section)comprising the steps of: providing a plurality of output signals (signal values from the signal generator to the scopes via the mux, pg. 630, right column, figure 1) from one or more blocks (covers a plurality of blocks, pg.627, right column, "To Manipulate Blocks" section, numbers 1-3); generating a composite signal comprising a set of the plurality of output signals ("plot your results in MATLAB after checking 'whos' to see all your outputs", pg.630, section 4. "Results" section, 1st paragraph); providing the composite signal as an output signal("plot your results in MATLAB after checking 'whos' to see all your outputs", pg.630, section 4. "Results" section, 1st paragraph); and storing the composite signal in a storage device (inherency since software is stored on a disk, computer etc.).

Claim 36. A method for graphically representing a composite signal in a modeling environment, (i.e., simulation, pg. 627, Preliminaries section)the method comprising the steps of: providing a plurality of output signals ("plot your results in MATLAB after checking 'whos' to see all your outputs", pg.630, section 4. "Results" section, 1st paragraph) from one or more blocks, each output signal graphically (pg.630, figure 3, "scope") indicated by a signal identifier; providing a composite signal identifier to graphically (pg.627, right column, bullet 8, "make hard copies of MATLAB plots) indicated a grouping of signal identifiers, the composite signal identifier representing a composite signal comprising a set of the plurality of output signals("plot your results in MATLAB after checking 'whos' to see all your outputs", pg.630, section 4. "Results"

section, 1st paragraph); and storing the composite signal identifier in a storage device (inherency since software is stored on a disk, computer etc.).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicants are advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 8, 9 and 15 and 27 were rejected under 35 U.S.C. 103(a) as being unpatentable over Dwan as applied to claims 1,14 and 27 above, and further in view of Austin et al.,titled, "Structure Matrix Computations with Units"; hereafter Austin. Dwan teaches most of the instant application above but fails to teach data structure data tree, network server residing in the Internet and m + n nodes.

Austin teaches

- Per claim 5 : list data structure (example of a row/column data structure, pg. 18, "Casting Units in Matrix Output")

- Per claims 8 and 9: a linked list data structure (pg. 25, line 15 and pg. 29, figure 11c, "Quantity Data Structure" and "Units Data Structure")

- Claim 9. the tree data structure(pg. 27, figure 10); including m+n nodes (pg. 38, lines 27 and 28 with pg. 19, "Addition and Subtraction" section).

- Claim 27: a network server residing in the Internet (pg. 2, Introduction, line 1).

Therefore, it would have been obvious to one having ordinary skill the art at the time the invention was made to utilize the Matlab software in Dwan in the data structure of Austin because Austin teaches a solution of self-contained and established problem

solving procedures, where the structure of a problem's input/output is well understood, identifying and correcting unintentional errors in the solution of new and innovative computations can be significantly easier when units are an integral part of the computation procedure (Austin: pg.3, lines 1-5).

Section III: Response to Arguments

101

9. Applicants are thanked for addressing this issue. Rejection is withdrawn.

1021/103

10. Applicants are thanked for addressing this issue. Rejection set forth in the previous final rejection have been amended with new art set forth above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicants' disclosure:

- Hiyama et al., "Matlab/Simulink based Transient Stability Simulation of Electric Power Systems" 1998 IEEE pg. 249-253: teaches a MATLAB/Simulink based transient simulation program.

- Davari et al., "On-line Control of a Real System with MATLAB/SIMULINK" 1998 Univ of W. Virginia pg. 7-9: teaches an interface routine using C programming language establishing communication betweeen MATLAB and an I/O card.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715.

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Anthony Knight 571-272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

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